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# MS-7313

Version 1.0

## CPU:

Intel Prescott ( L2=2MB ) - 3.4G & Above  
 Intel Cendar Mill (65nm) - 3.73G & Above  
 Intel Smithfield (90nm Dual core)  
 Intel Conroe (65W Dual core)

## System Chipset:

Intel Lakeport - MCH (North Bridge)  
 Intel ICH7R (South Bridge)

## On Board Chipset:

BIOS -- SPI  
 HD -- ALC888  
 LPC Super I/O -- F71882FG  
 LAN-- REALTEK RTL8111C Co-lay RTL8101E  
 CLOCK -- RTM876-665

## Main Memory:

DDR II \*2 (Max 4GB)

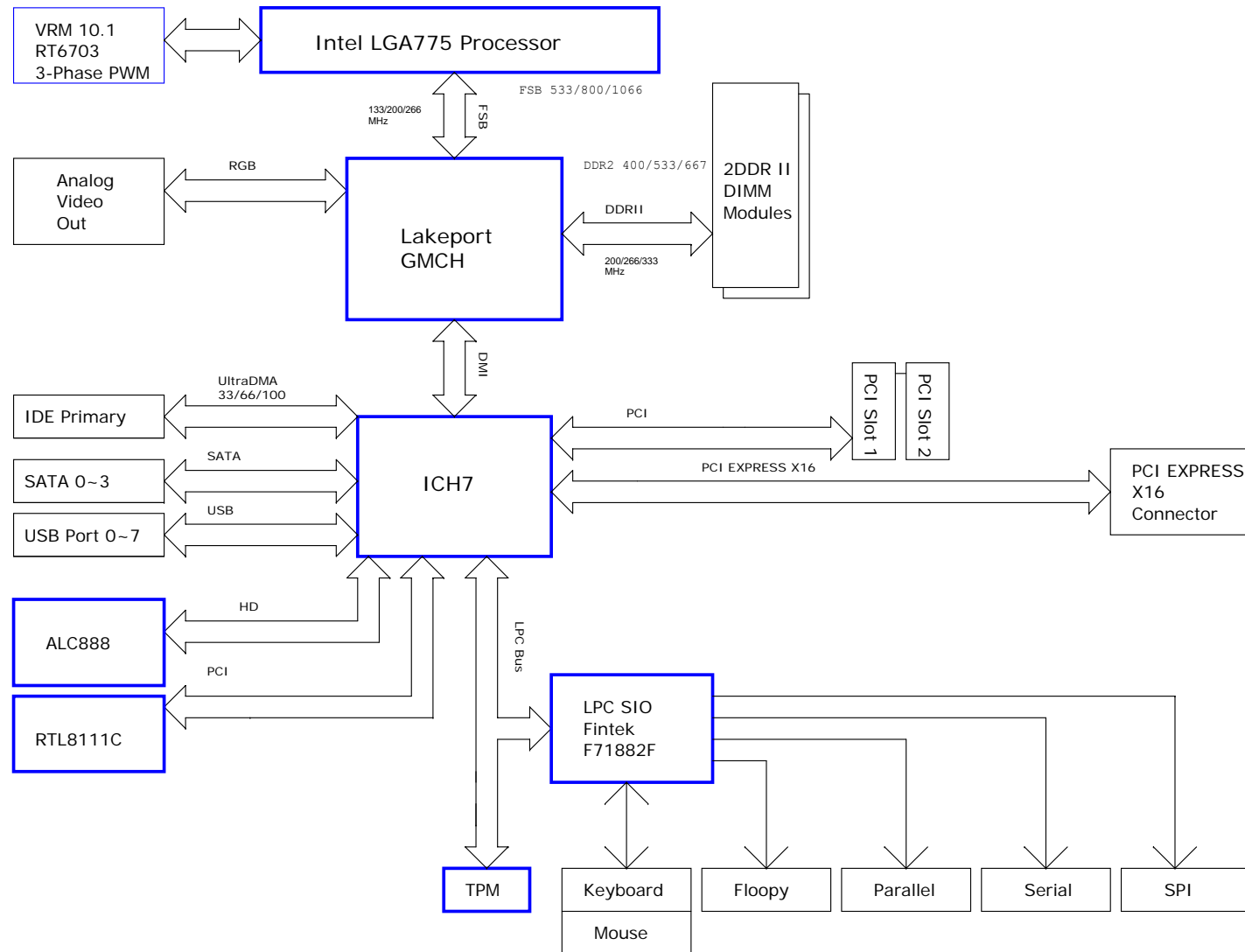
## Expansion Slots:

PCI2.3 SLOT \* 2  
 PCI EXPRESS X16 SLOT

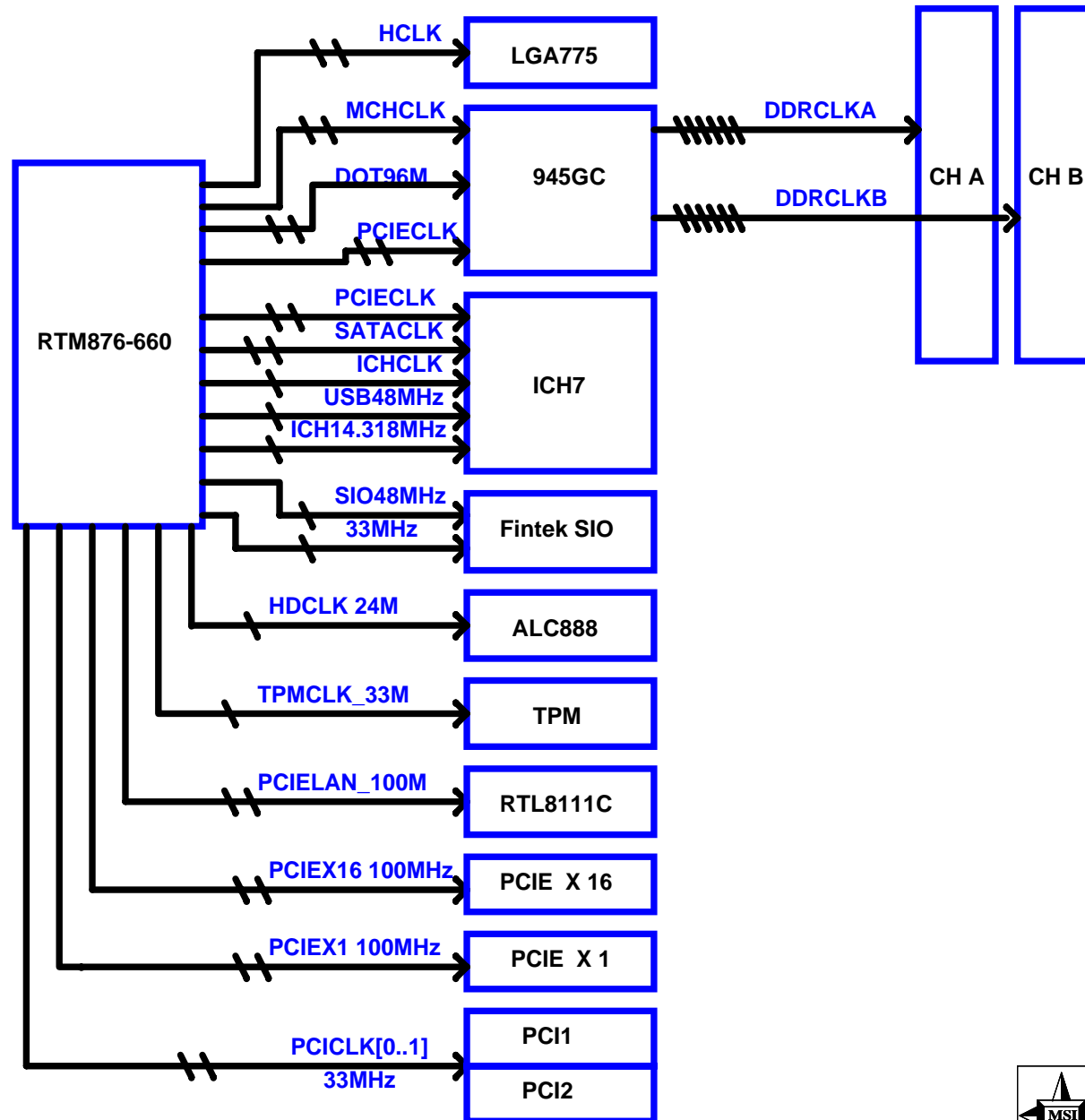
## ST PWM:

Controller: 3 PHASES

# Block Diagram



# CLOCK MAP



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MS-7313

Size Custom	Document Description <b>CLOCK MAP</b>	Rev 1.0
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<b>Processor</b>
0.8375-1.6000V Core-125A
1.2V FSB Vtt-5.3A
VCCPLL
VCC-IOPLL & VCCA

<b>945G/P MCH</b>
1.2V FSB Vtt-0.9A
1.8V DDR2 I/O-4.4A(S0,S1)
1.8V DDR2 I/O-25mA(S3)
0.9V DDR2 VREF-2mA
0.9V DDR2 SB_VREF-10uA
DDR2 Resister Comp V-36mA
DDR2 Resis Comp SB_V-10uA
1.5V Core-13.8A(Integrated)
1.5V Core-8.9A(Discrete)
1.5V PCI Express&DMI-1.5A
1.5V PCIE&DMI PLL-45mA
1.5V HOST PLL-45mA
1.5V VCCA_DPLLA&B-55mA
1.5V MPLL-66mA
2.5V DAC-70mA*
2.5V HV-3mA
2.5V CMOS-2.0mA

<b>ICH7</b>
1.2V VCC_CPU-14mA
1.05V Core-0.86A
VCC1_5A*-1.01A
VCC1_5B*-0.77A
5VRef-6mA
5VrefSus-10mA
+3.3V-0.33A
RTC-6uA(G3)
3.3V VccSus*-52mA
VccSus1_05V-See Note 1
VccUSBPLL-10mA
VccDMIPLL-50mA
VccSATAIPLL-50mA

Battery

<b>L6703 Regulator</b>
<b>VCCP</b>
0.8375-1.6000V

<b>VTT Regulator</b>
<b>V_FSB_VTT</b>
1.2V

<b>uP6103 Regulator</b>
<b>VCC_DDR</b>
1.8V

<b>uP6103 Regulator</b>
<b>V_1P5_CORE</b>
1.5V

<b>uP7707 Regulator</b>
<b>V_2P5_MCH</b>
2.5V

<b>1.05V Regulator</b>
<b>V_1P05_CORE</b>
1.05V

<b>uP7706 Regulator</b>
<b>3VSB</b>
3.3V

<b>uP7501 Regulator</b>
<b>5VDIMM</b>
5V

<b>W83310DS Regula</b>
<b>VTT_DDR</b>
0.9V

<b>DDR2 DIMM conn(4) &amp; term</b>
0.9V SM Vtt-1.2A(S0)
1.8V Vdd/vddq-4.7A(S0,S1)

<b>PCIE X16 slot(1)</b>
+12V-5.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

<b>PCIE X1 slot(1)</b>
+12V-0.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

<b>PCI slot slot(4)</b>
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-7.6A
+5.0V-5.0A
+12V-0.5A
-12V-0.1A

<b>USB</b>
+5V-4A(S0,S1)

<b>PS2</b>
+5V-345mA(S0,S1)

<b>CLKGEN</b>
+3.3V-560mA

<b>LAN</b>
3VSB-

<b>SIO</b>
+3.3V
3VSB-

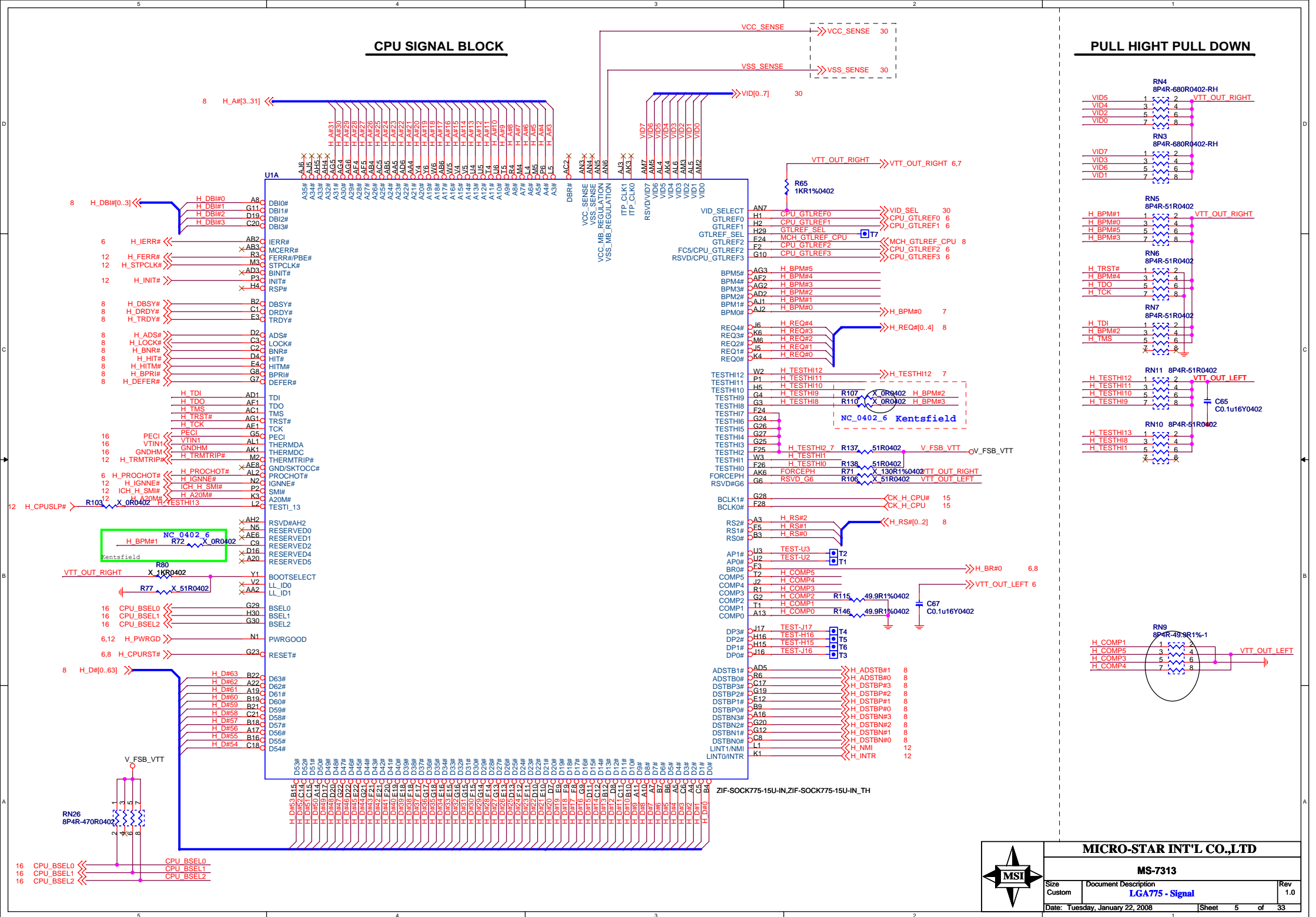
SPI ROM

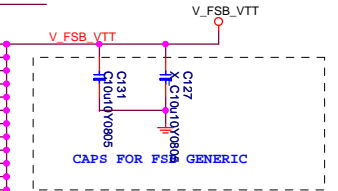
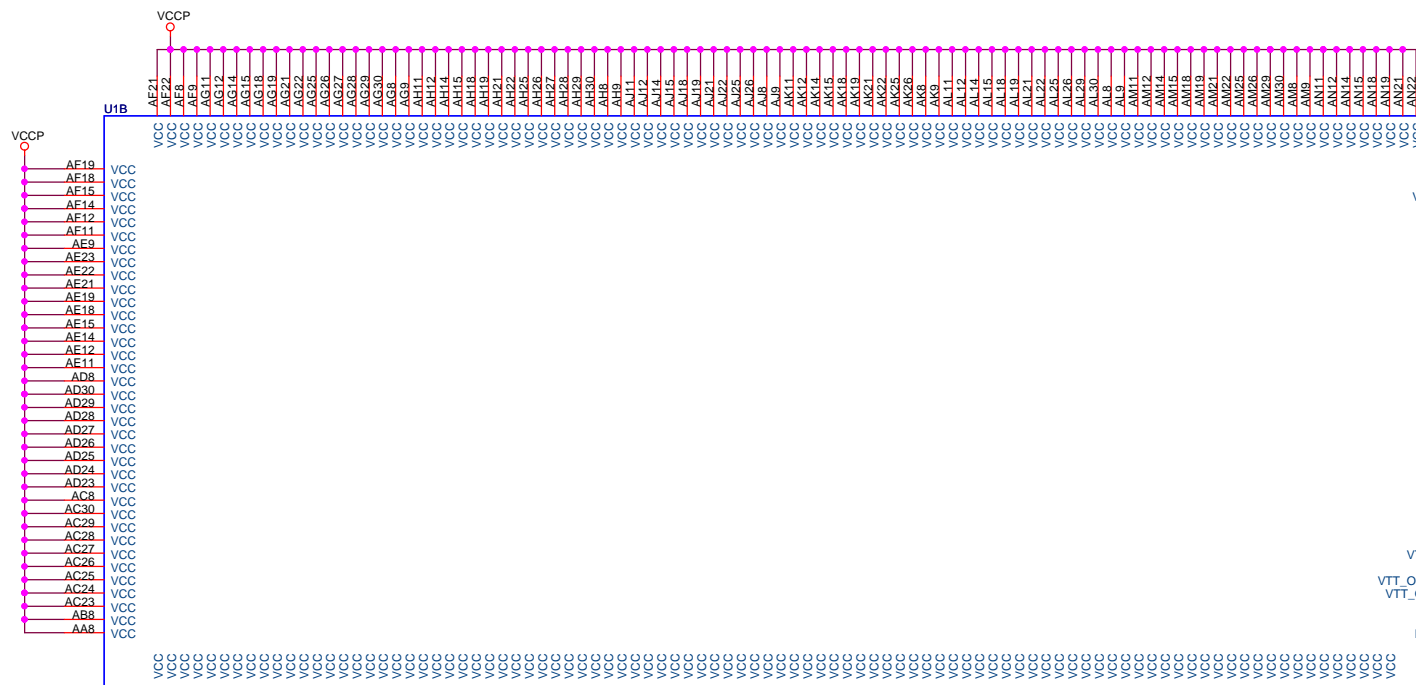
<b>Audio Codec</b>
--------------------

<b>1394</b>
-------------

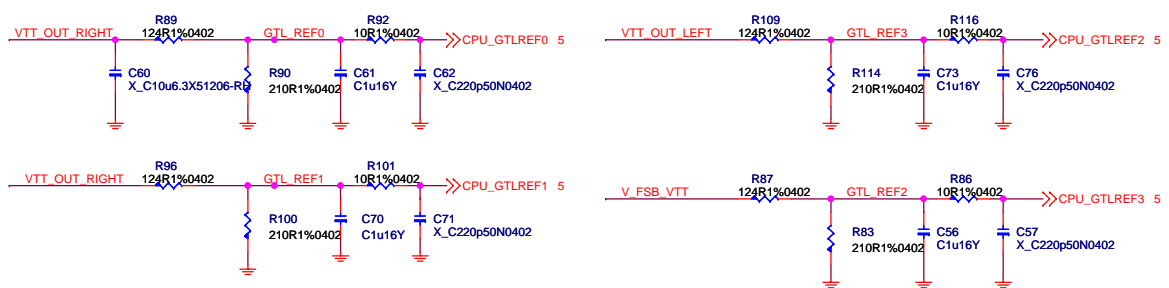
<b>+12V</b>
<b>ATX 2x2</b>

<b>+12V</b>	<b>+5V</b>	<b>+3.3V</b>	<b>+5VSB</b>
<b>ATX POWER</b>			

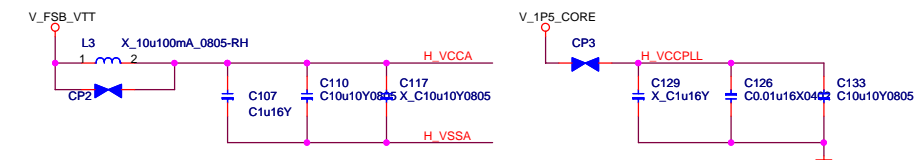




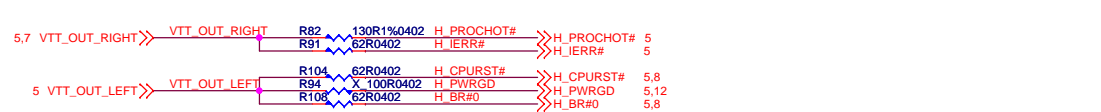
\*GTLREF VOLTAGE SHOULD BE 0.67 \* VTT = 0.8V (At VTT=1.2V)



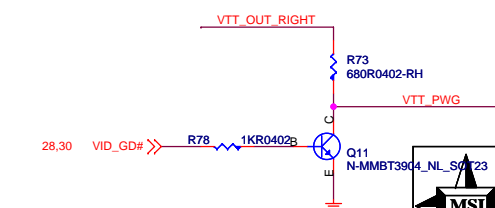
\*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET  
\*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS



PLACE AT CPU END OF ROUTE



### VTT\_PWRGOOD



VTT\_PWG SPEC :  
High > 0.9V  
Low < 0.3V  
Trise < 150ns

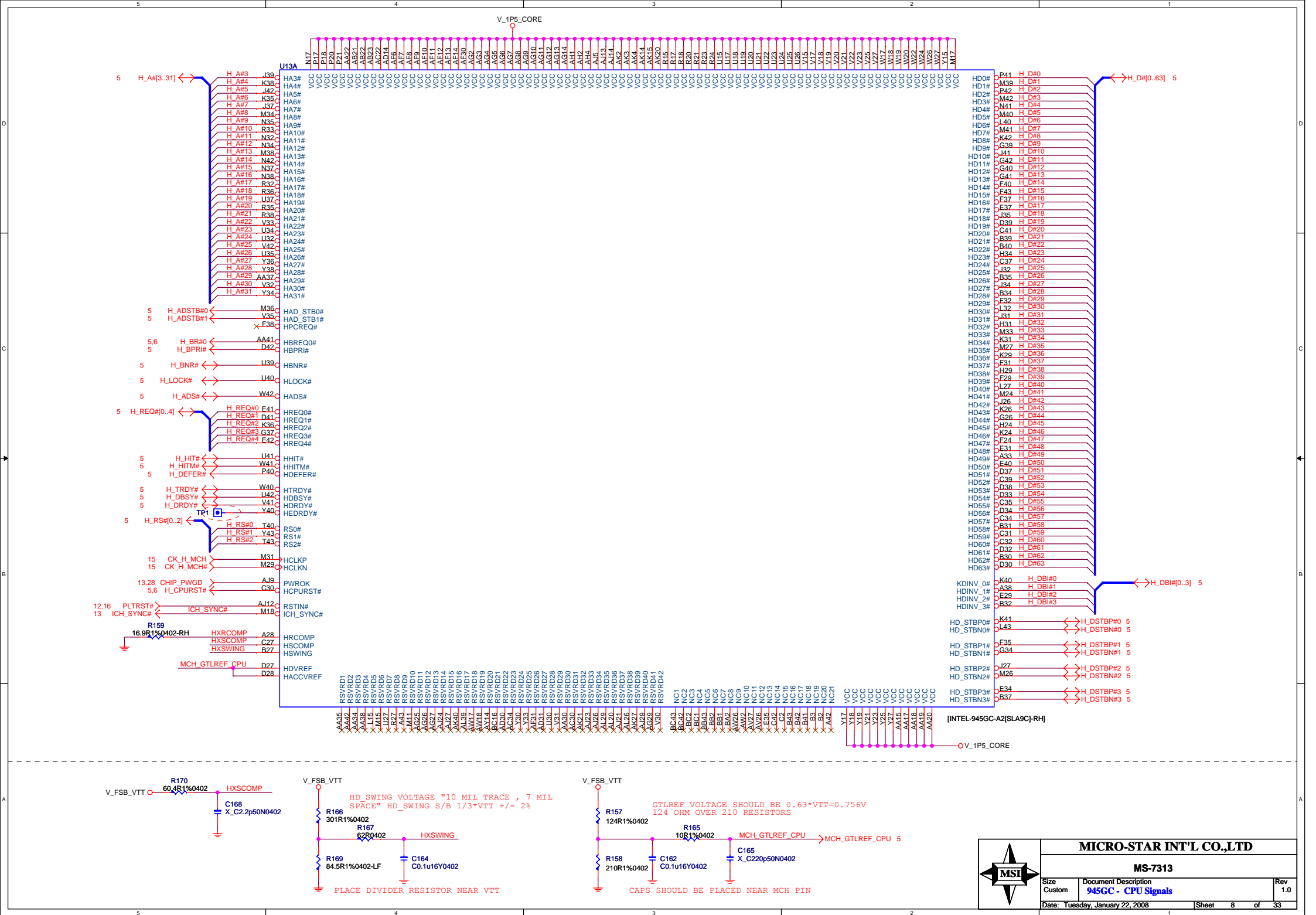
**MICRO-STAR INT'L CO.,LTD**

**MS-7313**

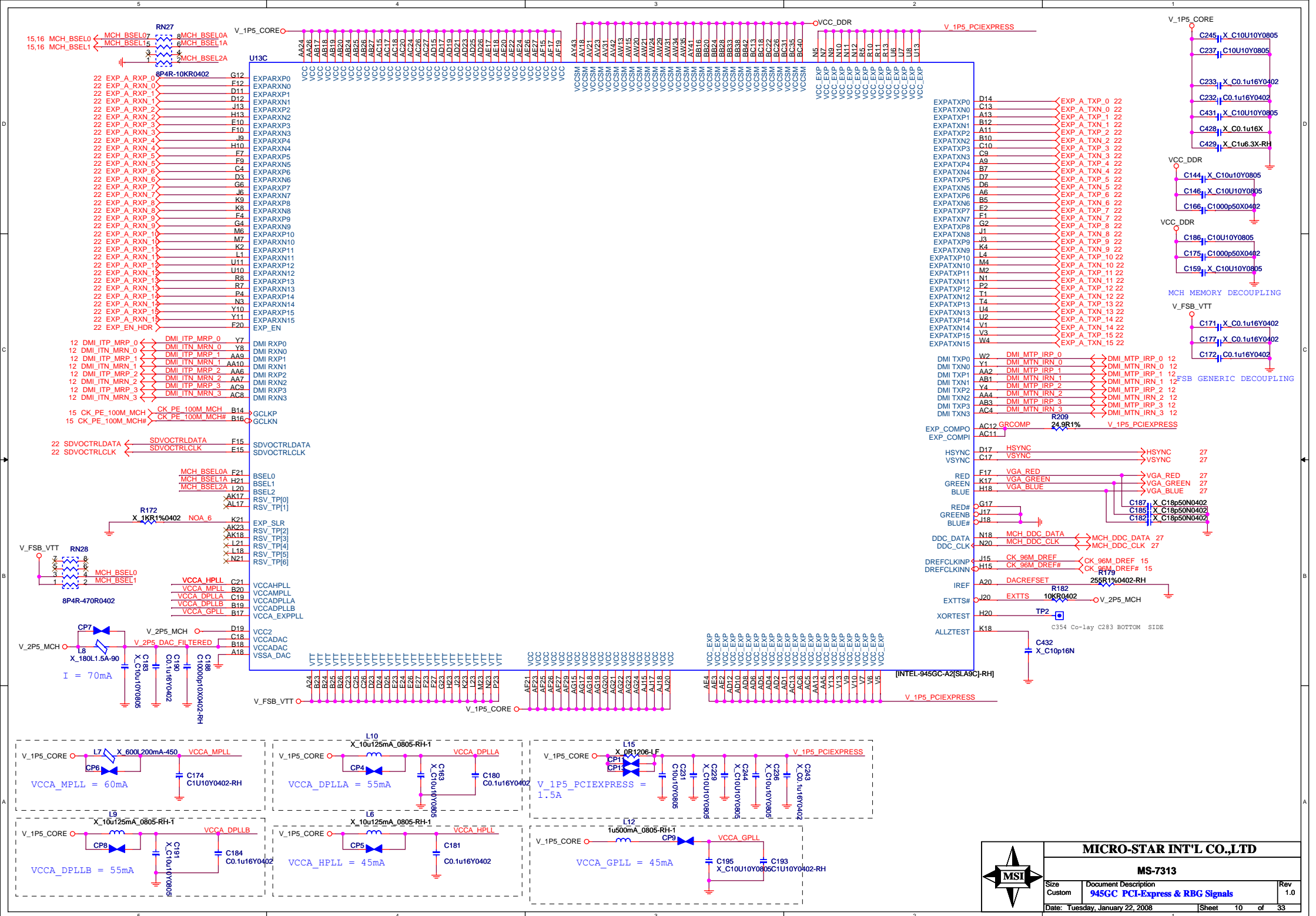
Size	Document Description	Rev
Custom	LG4775 - Power	1.0

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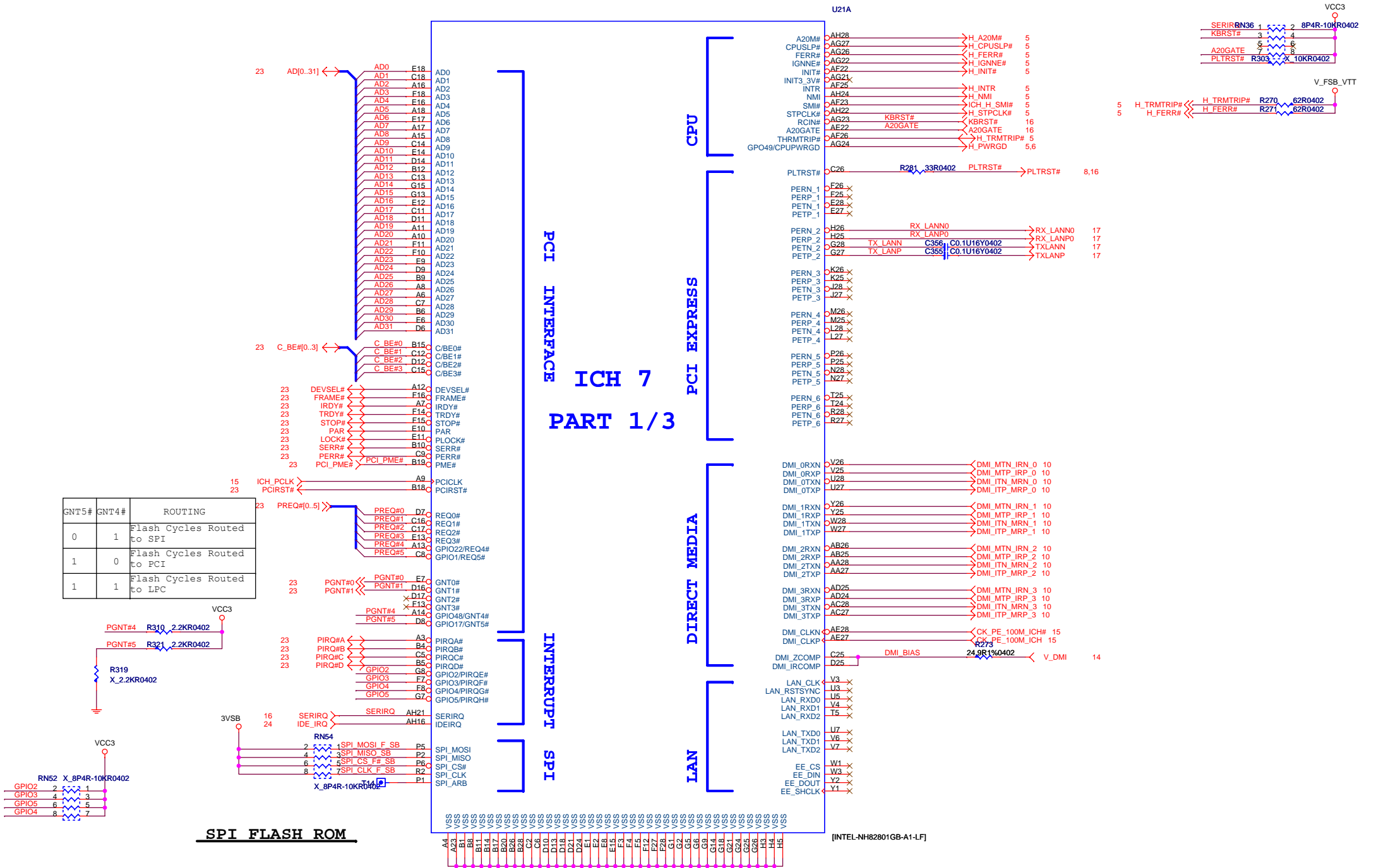









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Size	Document Description	Rev
Custom	Intel 945GC - GND	1.0
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GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC

**SPI FLASH ROM**

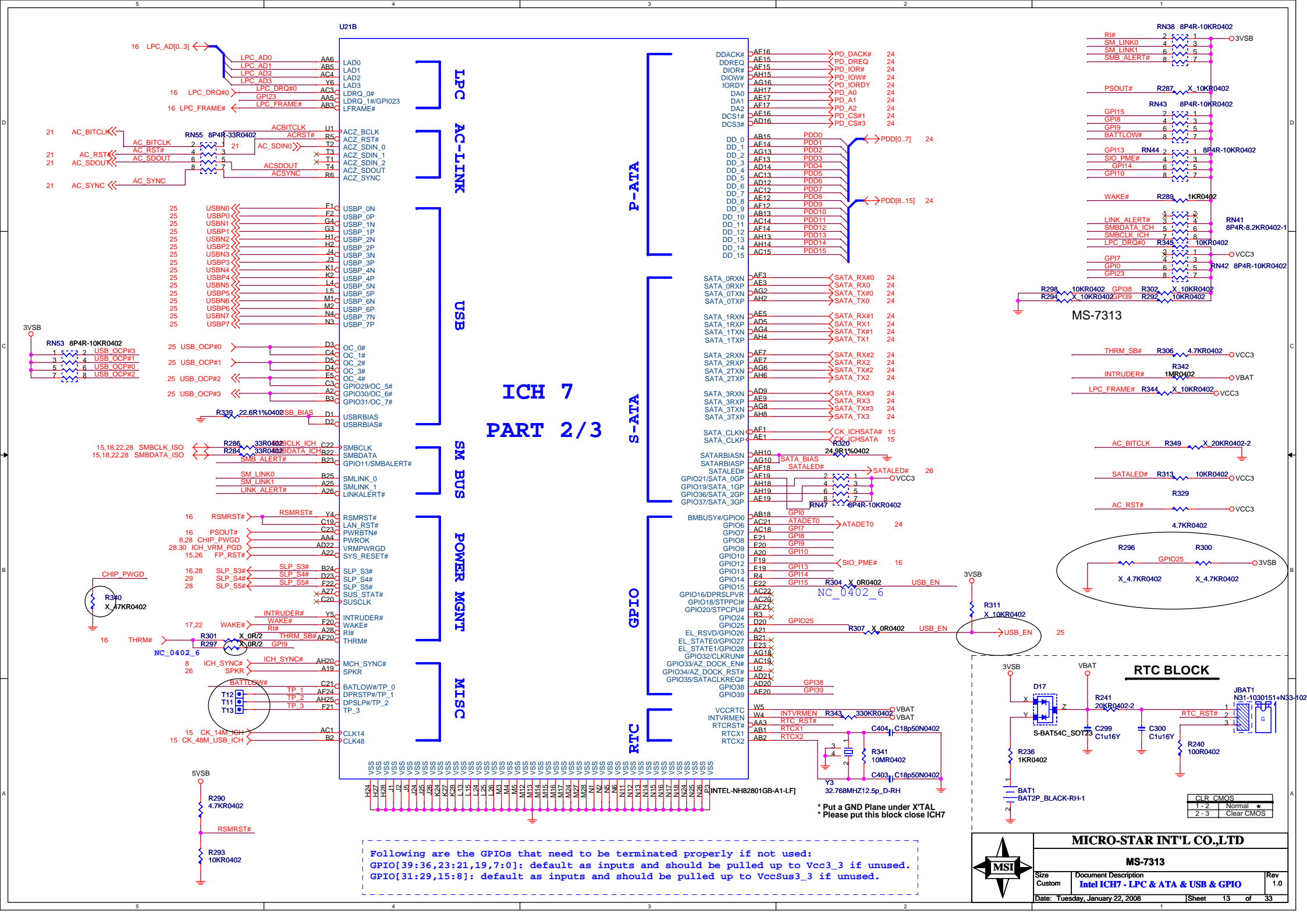


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**MS-7313**

Size Custom Document Description Intel ICH7 - PCI & DMI & CPU & IRQ Rev 1.0

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ICH 7  
PART 3/3

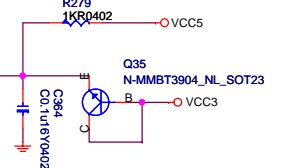
1.5V DMI POWER

1.5V CORE WELL POWER

S0 POWER

S5 POWER

5VREF Sequencing Circuit



[Intel-NH82801GB-A1-LF]

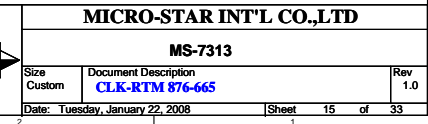


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Size	Document Description	Rev
Custom	Intel ICH7 - POWER	1.0
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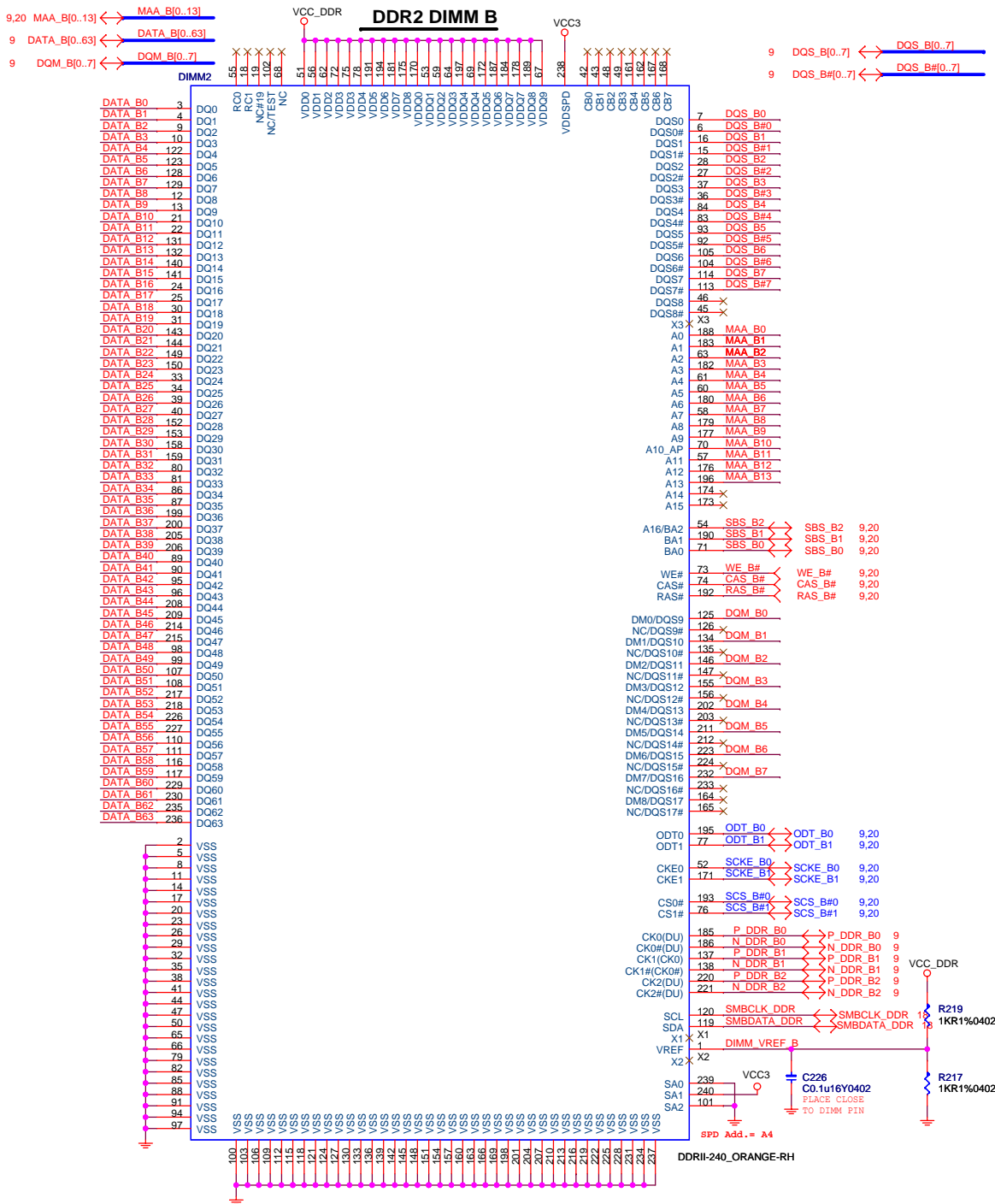
CPU Frequency Selection			
FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M









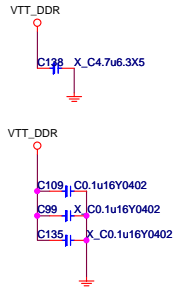


MICRO-STAR INT'L CO.,LTD

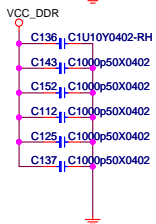
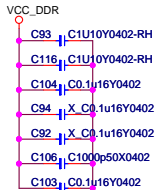
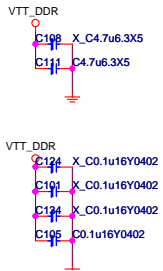
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Size	Document Description	Rev
Custom	DDR II DIMM A & B	1.0
Date:	Tuesday, January 22, 2008	Sheet 19 of 33

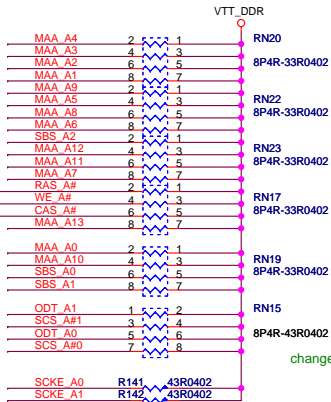
CHANNEL A V\_SM\_VTT DECOUPLING CAPS



CHANNEL B V\_SM\_VTT DECOUPLING CAPS



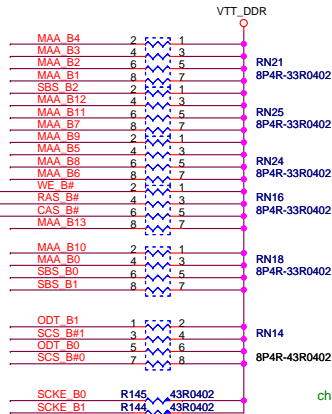
EMI



9,18 RAS\_A#  
9,18 WE\_A#  
9,18 CAS\_A#

9,18 MAA\_A[0..13]  
9,18 SBS\_A[0..2]  
9,18 SCS\_A#[0..1]  
9,18 SCKE\_A[0..1]  
9,18 ODT\_A[0..1]

change RN



9,19 WE\_B#  
9,19 RAS\_B#  
9,19 CAS\_B#

9,19 MAA\_B[0..13]  
9,19 SBS\_B[0..2]  
9,19 SCS\_B#[0..1]  
9,19 SCKE\_B[0..1]  
9,19 ODT\_B[0..1]

change RN

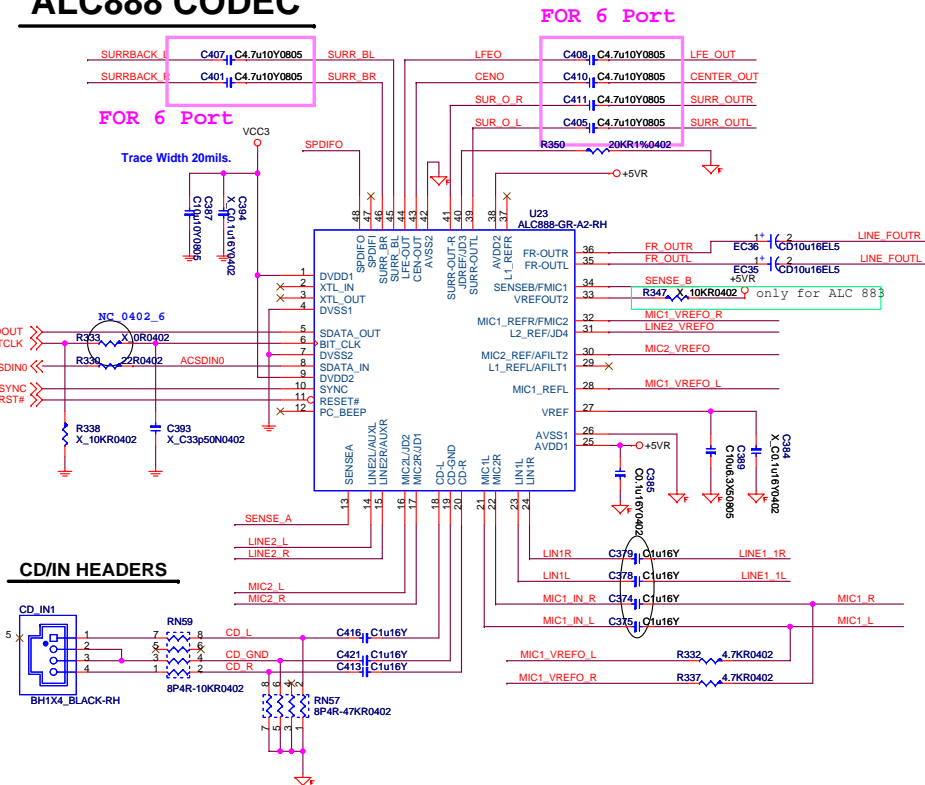


MICRO-STAR INT'L CO.,LTD

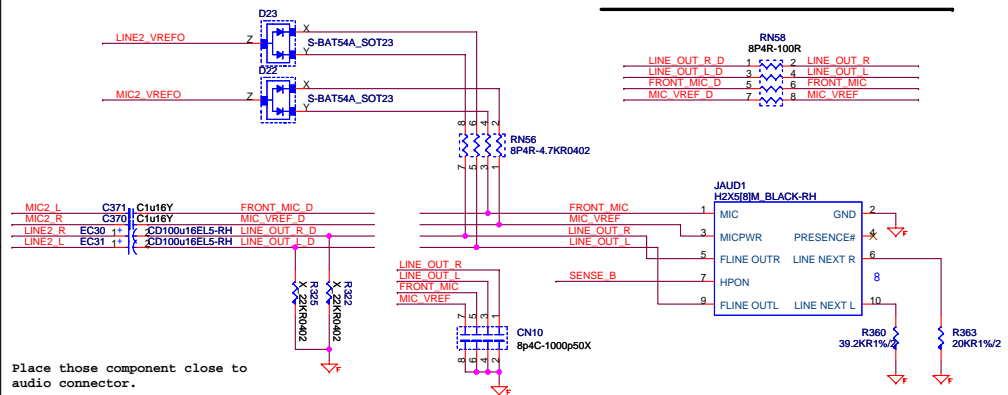
MS-7313

Size Custom	Document Description DDR II VTT DECOUPLING	Rev 1.0
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## ALC888 CODEC

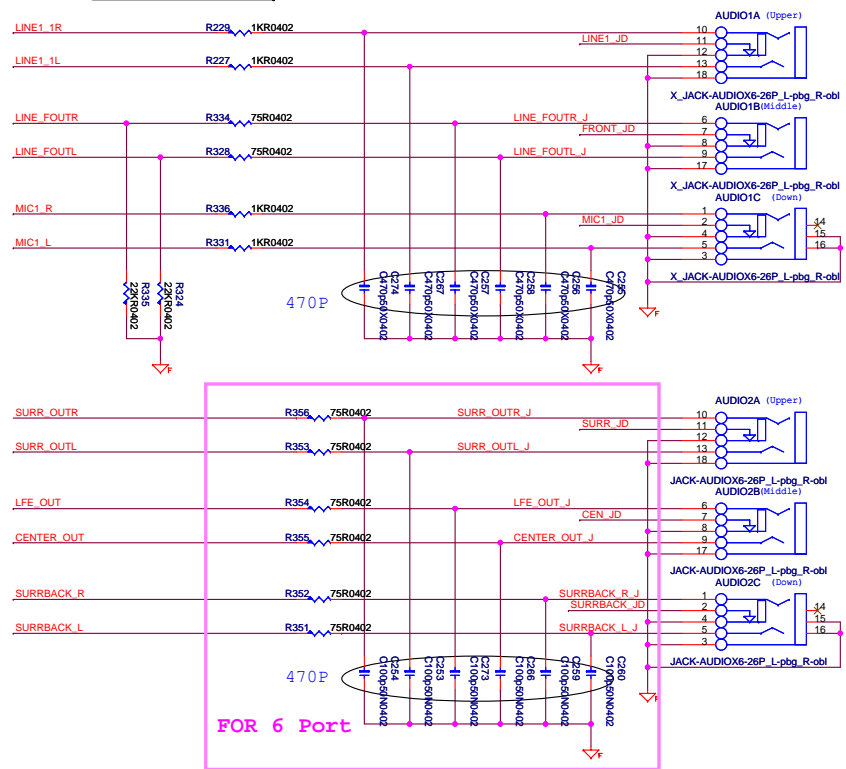


## Azalia Front Audio Connector

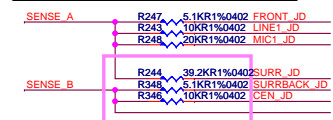


Place those component close to  
audio connector.

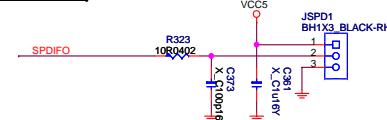
ALC888 JACK



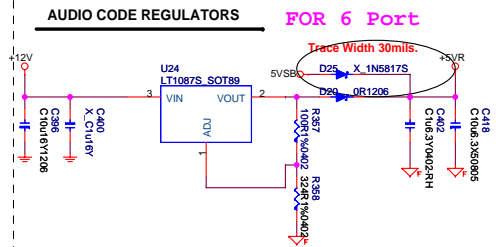
ALC883 JACK DETECT



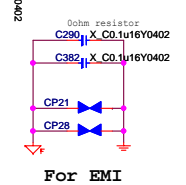
SPDIF OUT



## AUDIO CODE REGULATORS



FOR 6 Port



For EMI

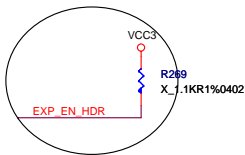
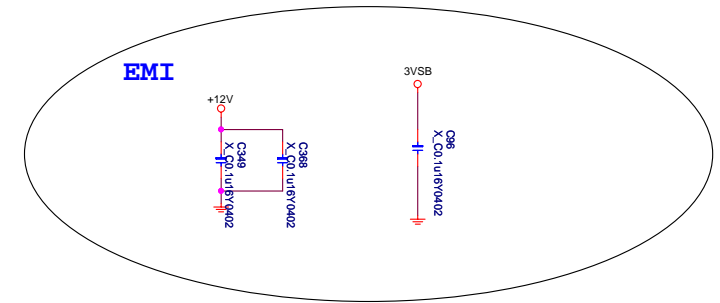
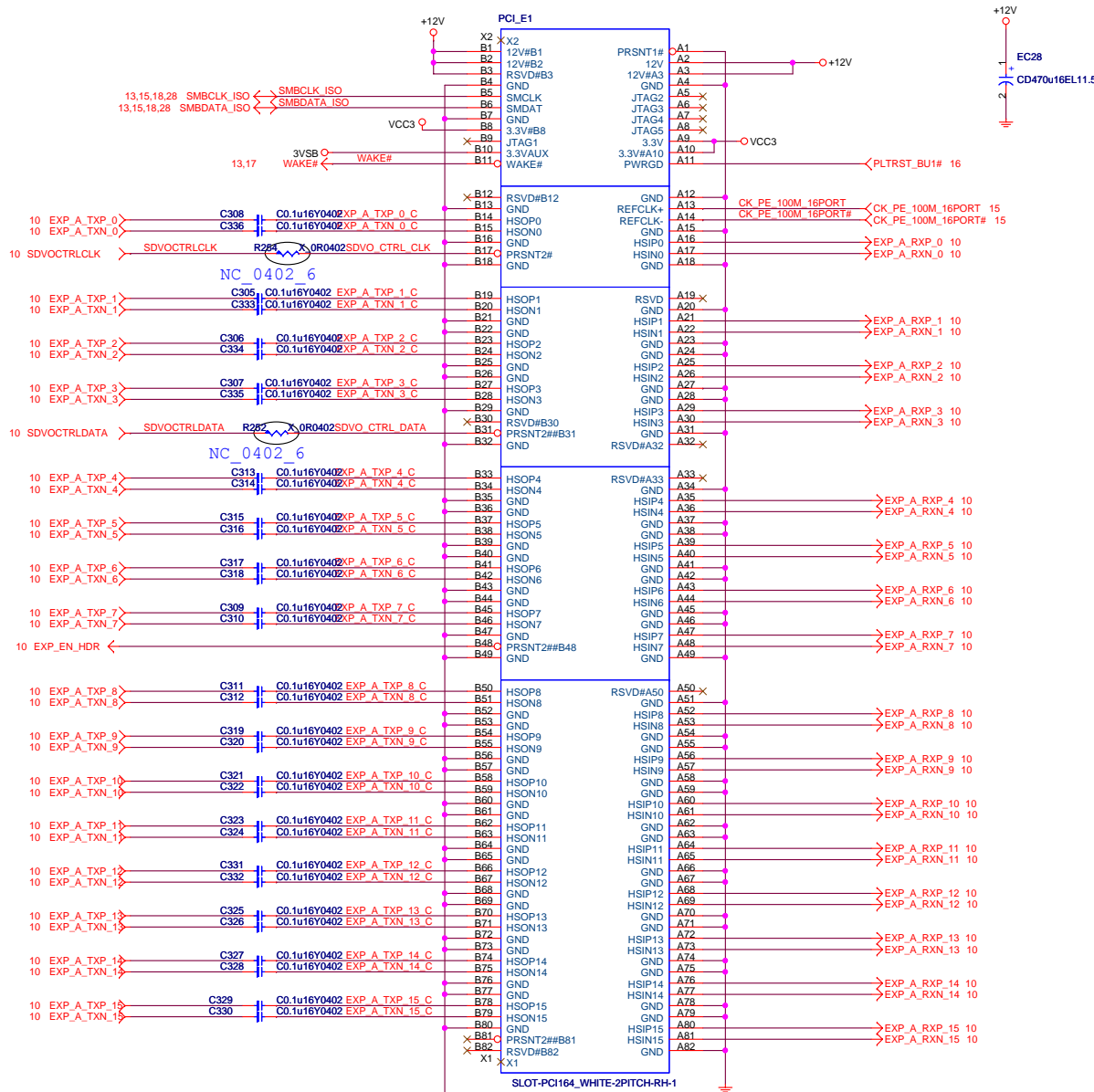


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MS-7313

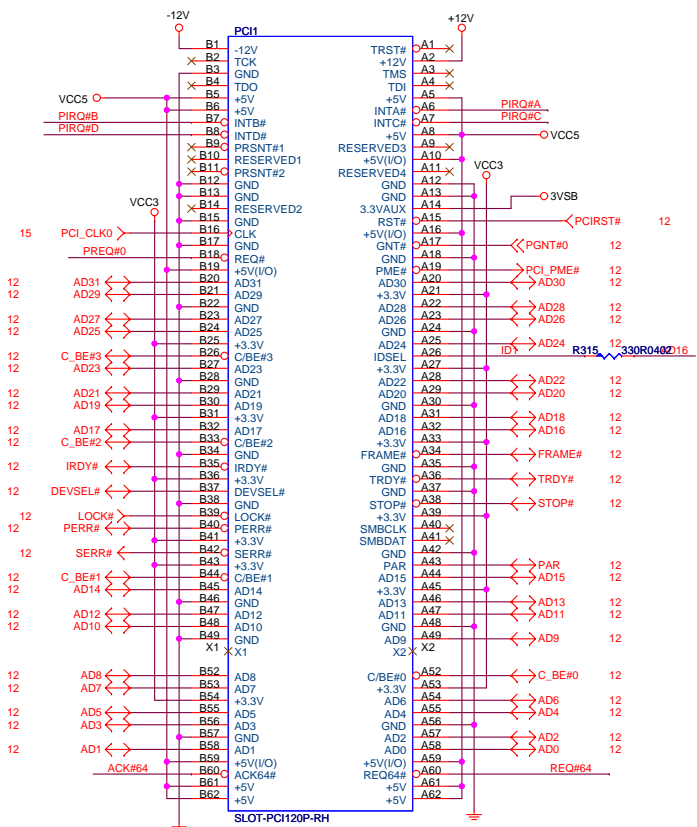
Size Custom	Document Description <b>21 HD ALC888</b>	Rev 1.0
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# PCIe X16 PORT



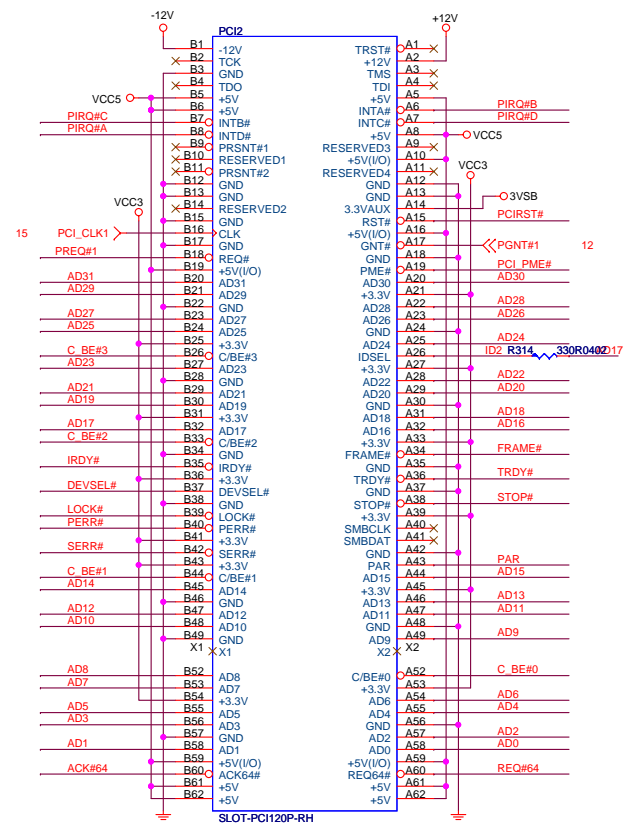
MICRO-STAR INT'L CO.,LTD			
MS-7313			
Size	Document Description	Rev	
Custom	PCI EXPRESSX16&X1	1.0	
Date: Tuesday, January 22, 2008	Sheet	22	of 33

# PCI SLOT 1 (PCI VER: 2.2 COMPLY)



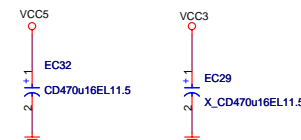
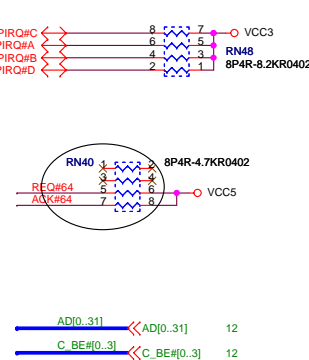
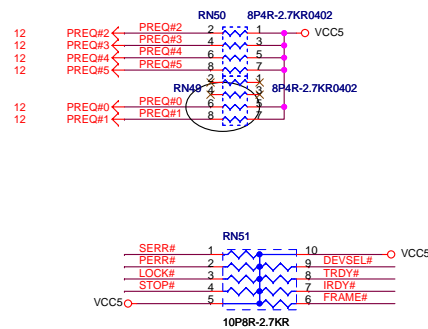
**IDSEL = AD16**  
**MASTER = PREQ#0**  
**PIRQ#A**

# PCI SLOT 2 (PCI VER: 2.2 COMPLY)



**IDSEL = AD17**  
**MASTER = PREQ#1**  
**PIRQ#B**

## PCI PULL-UP / DOWN RESISTORS

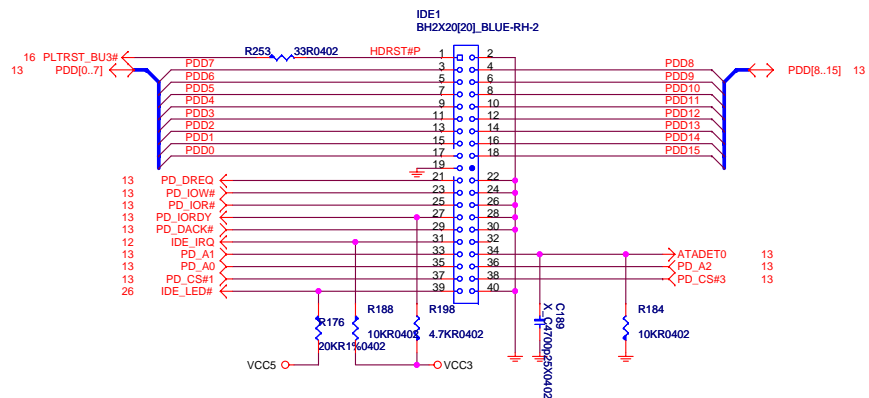


MICRO-STAR INT'L CO.,LTD

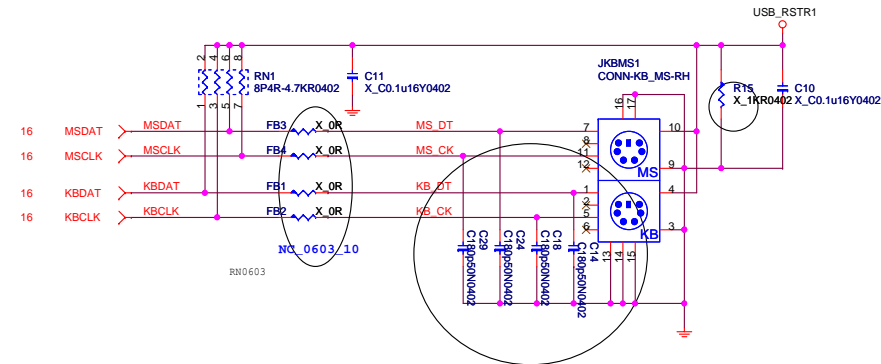
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Size	Document Description	Rev
Custom	PCI Slot 1 & 2	1.0
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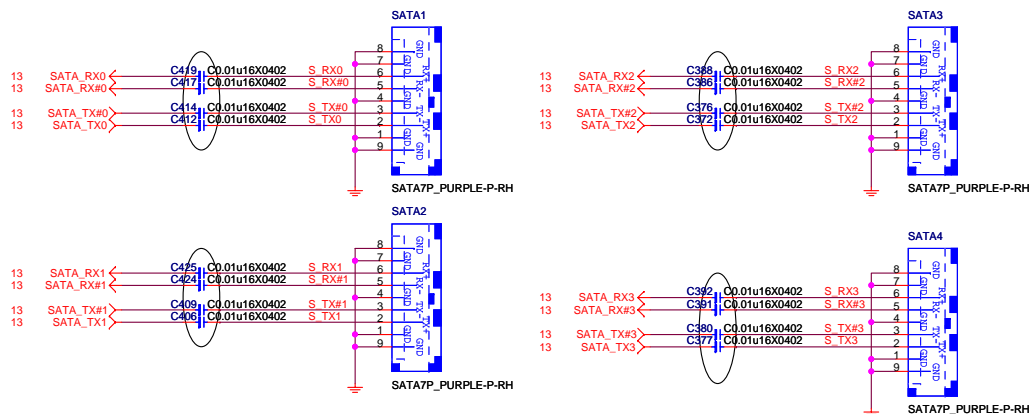
## ATA 33/66/100 IDE Connectors



## PS2 KEYBOARD & MOUSE CONNECTOR



## SERIAL ATA CONNECTOR BLOCK

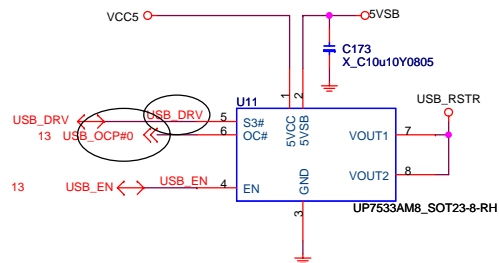


MICRO-STAR INT'L CO.,LTD

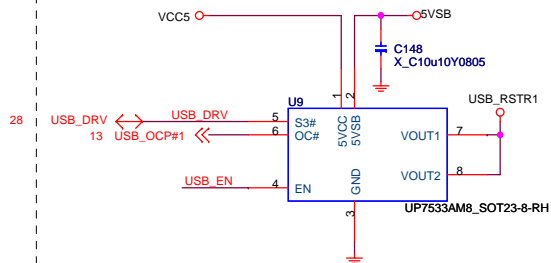
MS-7313

Size	Document Description	Rev
Custom	IDE & SATA Connectors	1.0
Date: Tuesday, January 22, 2008	Sheet 24 of 33	

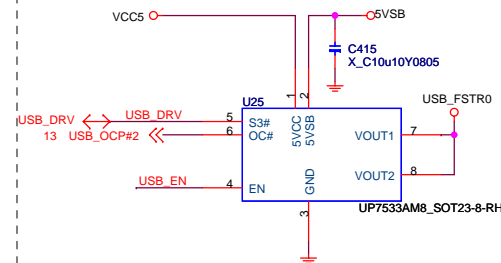
# POWER CIRCUIT FOR USB PORT 0,1



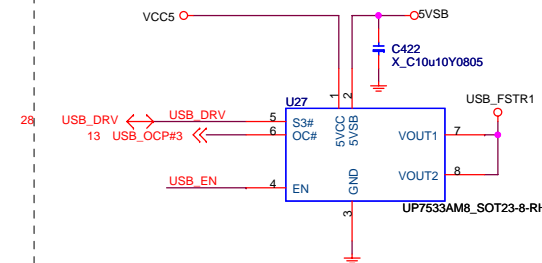
# POWER CIRCUIT FOR USB PORT 2,3



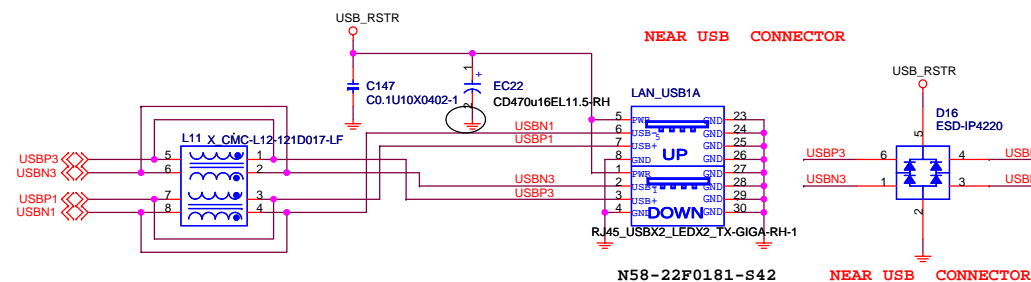
# POWER CIRCUIT FOR USB PORT 4,5



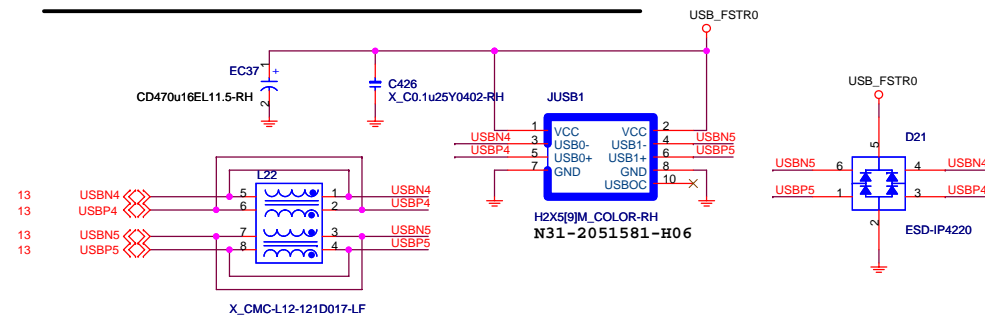
# POWER CIRCUIT FOR USB PORT 6,7



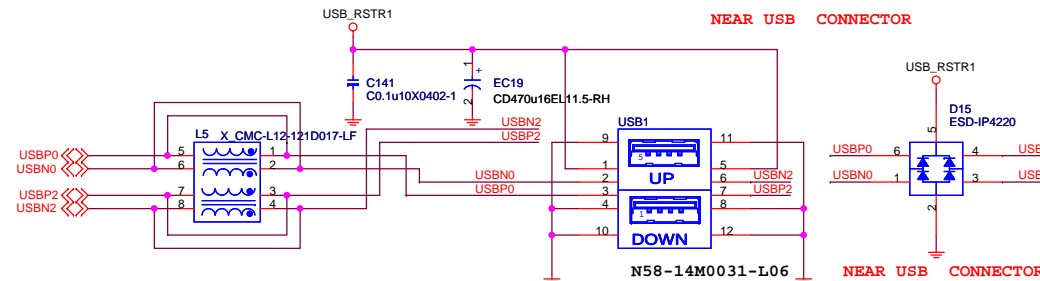
# REAR PANEL USB CONNECTOR FOR USB PORT 0,1



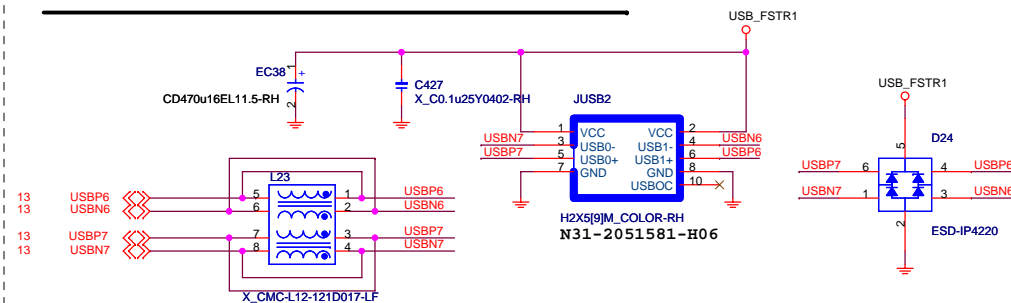
# FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



# REAR PANEL USB CONNECTOR FOR USB PORT 2,3



# FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



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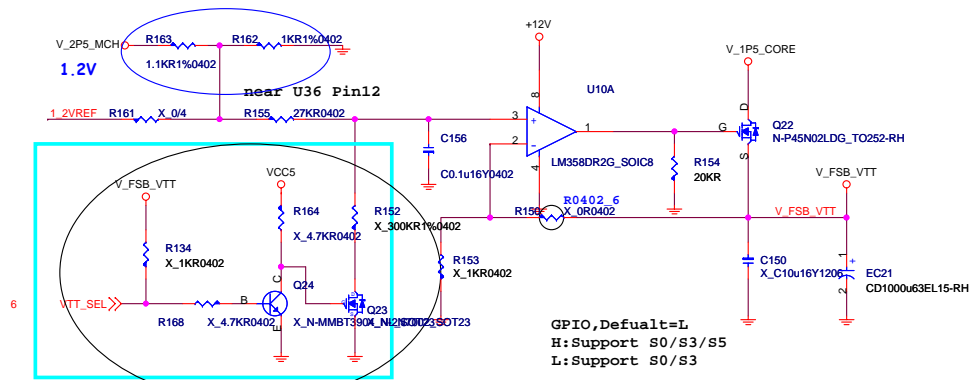
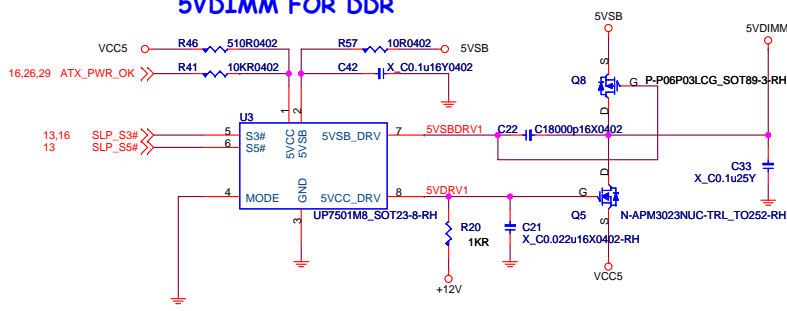
MS-7313

Size	Document Description	Rev
Custom	USB CONNECTORS	1.0
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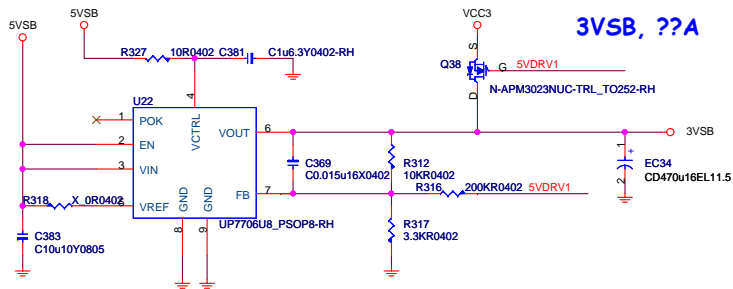


## 5VDIMM FOR DDR

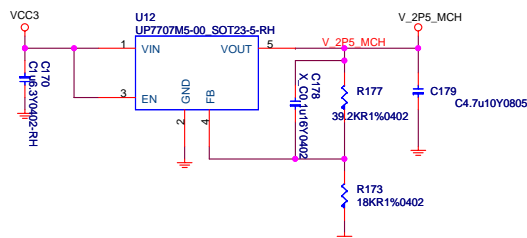


VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

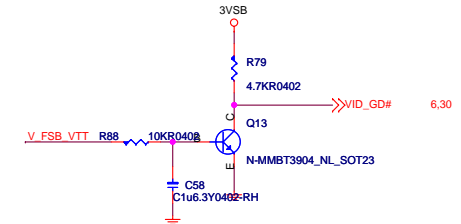
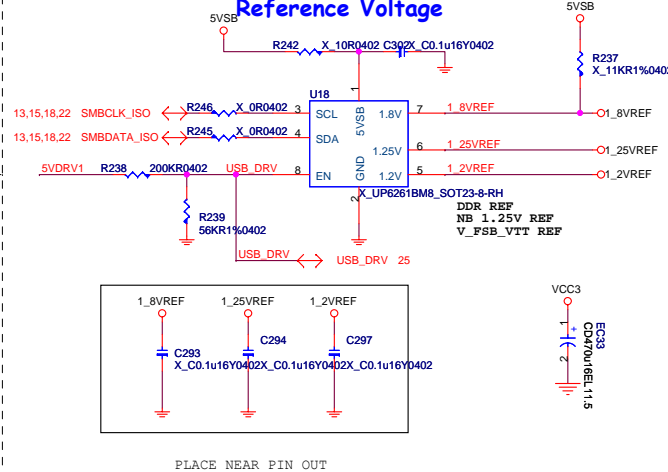
## 3VSB, ??A



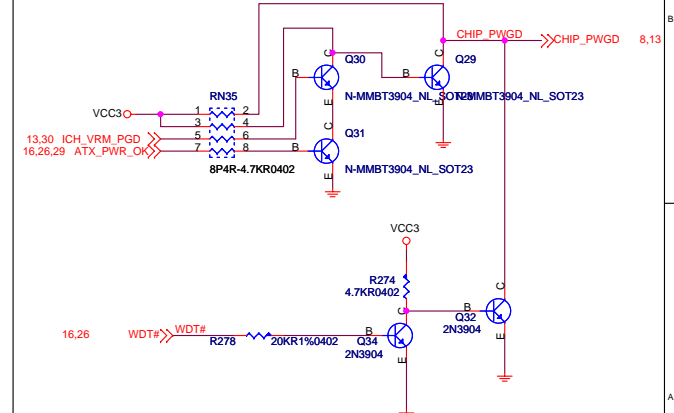
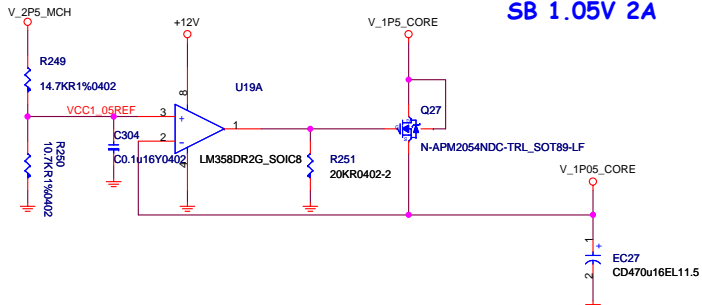
## V\_2P5\_MCH, 100mA



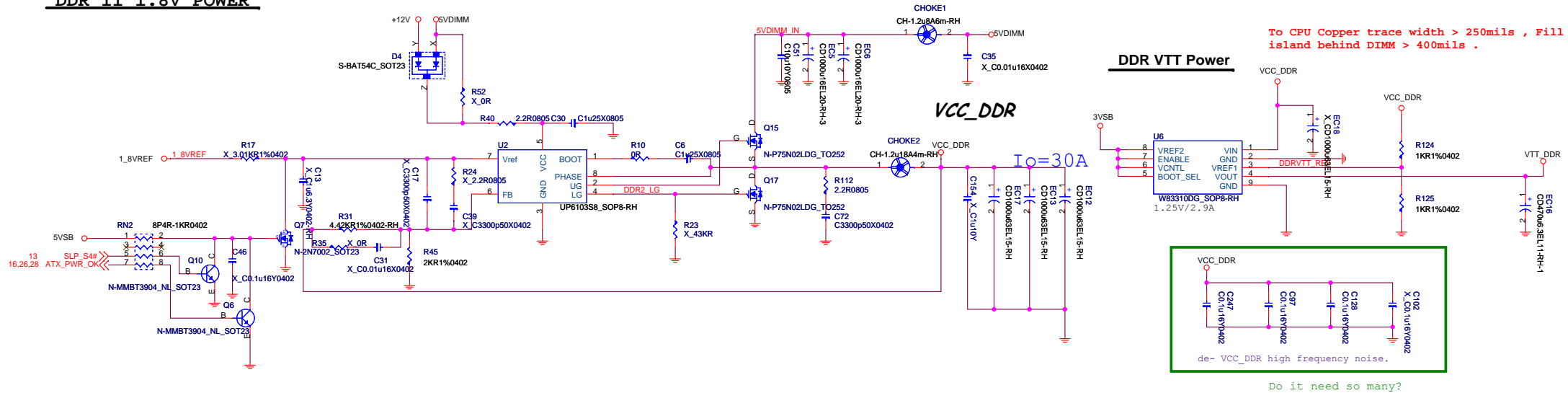
## Reference Voltage



## SB 1.05V 2A

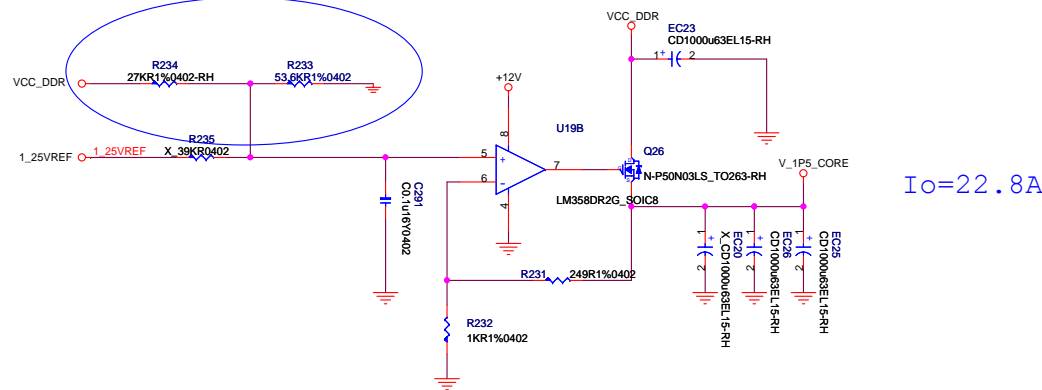


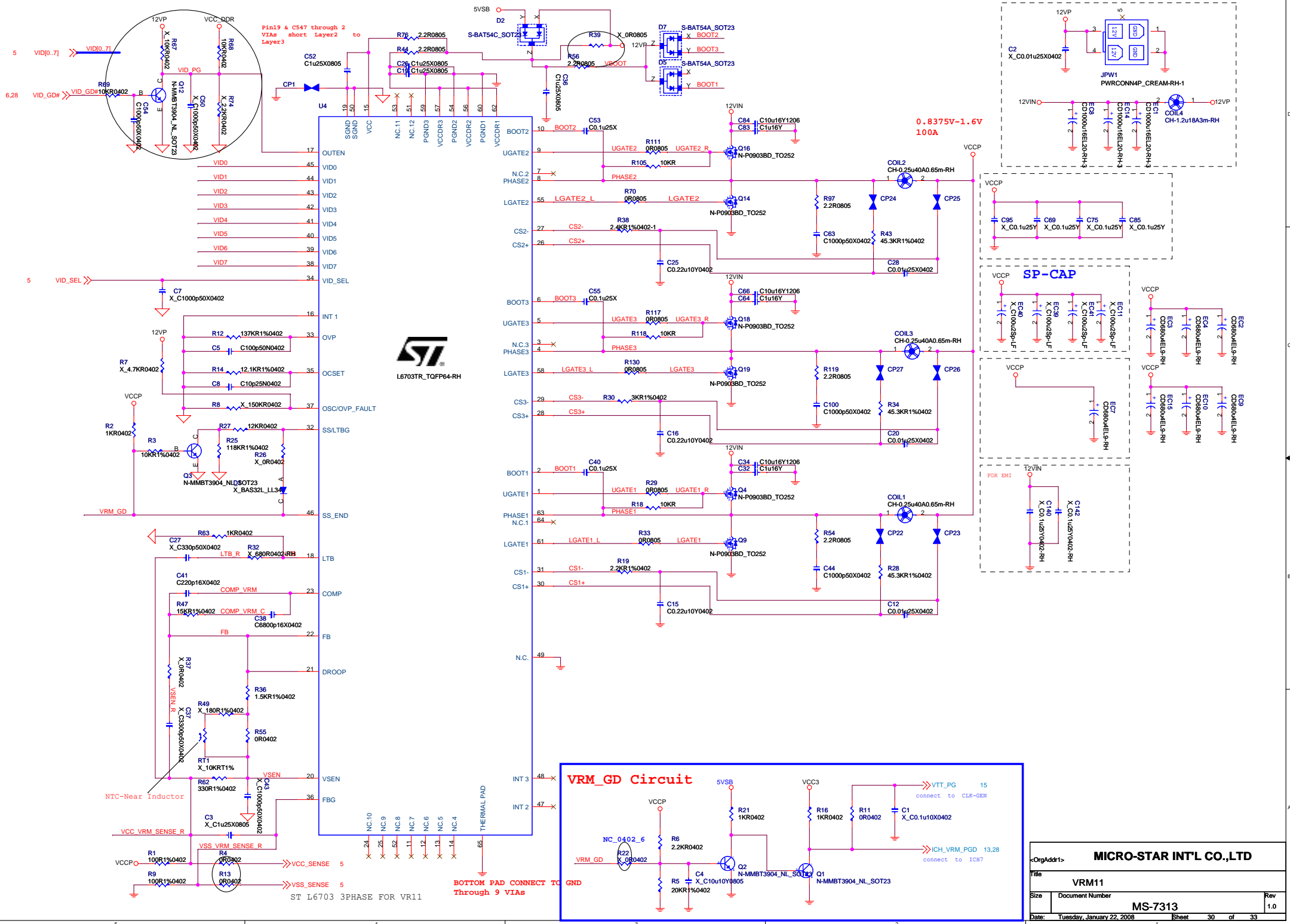
## DDR II 1.8V POWER



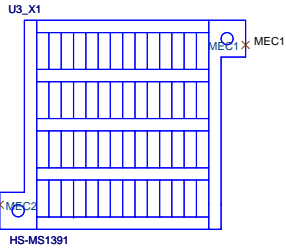
## 1.5V Core

For cost down

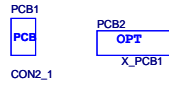
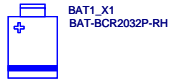
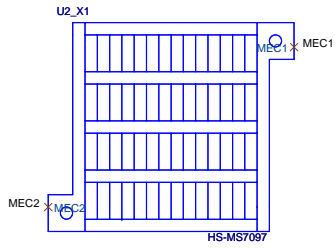




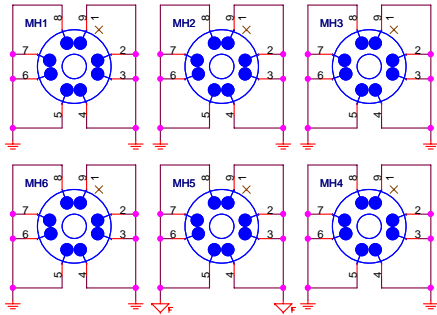
ICH7 HEATSINK



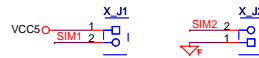
MCH HEATSINK



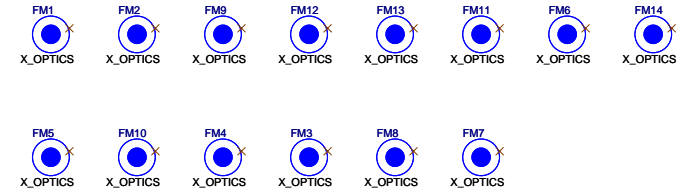
Mounting Holes



Simulation



Optics Orientation Holes



ICH7									
GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	<a href="#">GPIO(pull high)</a>
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	<a href="#">ATADET0</a>
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	<a href="#">SIO_PME#</a>
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	<a href="#">BIOS_WP#(fill with 1)</a>
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD
Following are the GPIOs that need to be terminated properly if not used: GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused. GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.									

SIO Fintek71882FG(CONTINUE)

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OD12t	
GPIO6	SLOT0CC#	55	GPO	I/OD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OD12t	

PCI Config.

DEVICES	MCP1 INT	PIN REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JUMPER SETTING

<b>JBAT1</b>	<b>(1-2)NORMAL</b>	<b>(2-3)CLEAR</b>
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File BIOS Request Form		
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0A Change list:

- 1.Remove 1394 & PCIE-X1;
- 2.modify usb1
- 3.Remove EC18,EC19,EC57,EC62,D19, D22, D24, D25; R87,R91,R92,R96
- 4.5VREF Change 5817 to 3904
- 6.Change DDR Chock to 8A, 18A
- 7.LAN的EEPROM部分: R201,U29,R213不上件;
- 8.合并LED\_VCC,LED\_VSB两个信号电阻为排阻; ICH\_VRM\_PGD;ATX\_PWR\_OK两个信号电阻为排阻
- 9.Modify page NO. and off page ;
- 10.Change EC64,EC65,EC88 TO MLCC C76 , C77 , C85
- 11.Change audio 6 Port to 3 Port
- 12.power circuit update :R372 上件, RT3 & R244不上件
- 13.remove D52 , change C278 to 0805 10U
- 14.For EMI Request:remove C91 ,ADD 2 pcs VCC\_DDR-VTT\_DDR 0.1uf cap : C262 C266 ;  
ADD CTRL18-GND 0.1ufcap: C221 , AVDD33-GND 0.1uf cap:C230 , AVDD18-GND 0.1ufcap: C219
- 15.Modify LPT:remove D7,D8 ;change 8P4R to 10P8R RN74,RN75;
- 16.Modify PCI RN39,RN40 8P4R to RN76 10P8R AND remove c148, c187 for EMI;
- 17.统一 USB CONNECTOR netname

For CostDown

- 18.Delet: EC33,EC35 (VCC5) for USB power;EC31 for 3VSB power;EC45 for 5VCC power;EC49,EC89 for 3VCC power
- 19.Delet EC68 (VCCP) for power team ; Change H/L-mos to D03-0903BDB-N03 H-MOS, D03-75N022B-N03 L-MOS
- 20.Change EC40 to C616(1206) ; C608,C609 change to 1206
- 21.Change Q17 TO252 to SOT\_89
- 22.Remove C206,C267,C238,RN16 ,R265,R266,C138; Change C237,C601 22uf to 10uf;  
Remove R118,R119 USE RN31; Remove R384,R388,R389 USE RN77;
- 23.Change R215 0805 to 0603 ,Remove C269, R226 ,R75; Change L-mos D03-75N022B-N03 to D03-0903BDB-N03;  
Remove R163,RT1,Stuff Q19 for system Tem;  
RemoveC173,C224,C56,C57,C58
- 24.Delet Q26,R393,R202,Q42,R343,C277,R168,Q43,C276,C276,D19,R435,R161
- 25.Remove U9,U10,And stuff R479,R480 for VGA; Remove C189,C200,C271
- 26.Swap JUSB1 PIN and LPT PIN ,Delet EC12 for Power Team,Delet c224 C186;  
Delet R400 R403 R406 change to line,Delet R335 C266 D28 CP34 C229 C345 C465 C109 C148 CP48 C43 CP27 CP28
- 27.Dealet CP32 CP46 For EMI ,Rename ,Delet C23 for power team ,Change R171 0603 to 0402
- 28.Change PGND to GND For EMI
- 28.Change X\_J2 GND to GNDF For LAYOUT

Title			
History			
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